

ky diodes D_1 and D_2 allow you to power the ICs using the input voltage until the output rises, at which time the higher output voltage powers the ICs. C_{DC} is a storage and decoupling capacitor for this power bus. The higher power-supply voltage is necessary for proper operation, and it lowers the on-resistance of the analog switches. The 0.4Ω on-resistance of IC_1 results in low circuit losses and high-efficiency operation. IC_1 , IC_2 , and IC_3 exhibit a break-before-make operation, which is essential in this case.

For a 50%-duty-cycle clock, you can calculate the theoretical power-efficiency of the converter, according to the

following equation:

$$\eta \approx 1 - \left(\frac{1}{2} + \frac{\frac{C_{OUT}}{3C}}{\left(1 + \frac{C_{OUT}}{3C}\right)^2} \right) \times \frac{1}{12R_L C F}$$

If the value of C_{OUT} is equal to the value of C , the power loss due to charging of the three capacitors is about two-thirds of the power loss during the discharging phase. The power consumption of the control circuit reduces the efficiency of this calculated value. For CMOS circuits, the power consumption rises linearly with the operating frequency. By choos-

ing the operating frequency, you can optimize the efficiency of the circuit. The optimum frequency is inversely proportional to the load resistance, R_L . Fortunately, the efficiency maximum is flat, so you can achieve efficiencies higher than 90% over a wide range of values for R_L . You can attain 94% efficiency driving a 120Ω load over clock frequencies of 100 to 400 kHz. If you set a 229-kHz operating frequency, an input of 2.2V yields a 2.87V output at an efficiency of 95.9%. The optimum clock frequency shifts to lower values at lighter loads. You can drive a 269Ω load at 100 kHz and achieve an output of 2.88V. **EDN**

Bootstrap circuit speeds solenoid actuation

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The circuit in this Design Idea bootstraps a large capacitor in series with the solenoid to provide a large actuation voltage (Figure 1). This higher voltage provides substantially more current to operate the solenoid (Figure 2, which is available at www.edn.com/100610dib), speeding the operation of the solenoid. You can also choose operating voltages or solenoid specifications that result in lower continuous current through the solenoid, reducing

dc power consumption and resulting in a cooler-running solenoid with better reliability.

When there is a 0V input to the circuit, both transistors are off. Resistor R_1 slowly charges the left side of capacitor C_1 to the 24V power-supply voltage. D_2 clamps the right side of capacitor C_1 to 0.6V. When the input signal goes high, both the Q_1 and the Q_2 transistors turn on. This action quickly drives the left side of C_1 to ground. Because voltage

THE TIME CONSTANT DEPENDS ON THE SOLENOID'S INDUCTANCE AND THE CAPACITOR'S VALUE.

cannot change instantaneously across a capacitor, the right side of C_1 goes down to -23.4V. D_2 steers the solenoid current into the capacitor until it discharges, at which time the solenoid current conducts through D_2 to ground. D_1 prevents a voltage-overshoot spike when the circuit turns off, and current suddenly stops flowing in D_1 . It clamps the bottom leg of the solenoid to 24.6V until the current decays in the solenoid.

The time constant of the circuit depends on the inductance of the solenoid and the value you choose for the capacitor, which you can calculate with the following equations:

$$I(t) = \frac{(2V_{IN} - V_D)}{\omega L} e^{\left(-\frac{t}{\tau}\right)} \sinh(\omega t);$$

$$\omega = \sqrt{\left(\frac{R}{2L}\right)^2 - \frac{1}{LC}}; \text{ and } \tau = \frac{2L}{R}.$$

In these equations, e is the mathematical constant, ω is the radian angular frequency, and t is time in seconds. In addition, L is inductance and R is resistance. **EDN**

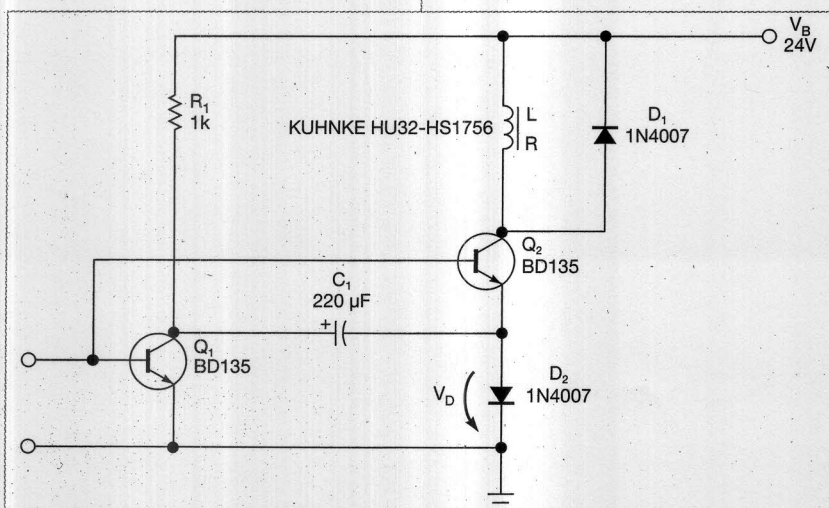


Figure 1 This circuit bootstraps the power supply voltage across the solenoid to temporarily double the actuation voltage.